

## ABSTRACT

The specification discloses a structure of and a method of operating a subtractive division (SD) cell where a portion of the partial remainder or estimated partial remainder directly indicates the next quotient digit. More particularly, by sufficiently constraining the prescaled range for each possible divisor, only a few bits of the partial remainder (the exact number dependent upon the radix), along with their related carries (if any), directly indicate the value of the next quotient digit. Because fewer bits of the partial remainder are needed to make this determination than needed in related art devices, and further because no look-up table or hard-coded decision tree is required, calculation time within each SD cell is shorter than related art devices. Having a shorter calculation time within each SD cell allows for either completion of a greater number of SD cells within each clock cycle, or completion of the calculation to full precision in less time.

10  
20  
30  
40  
50  
60  
70  
80  
90  
100  
110  
120  
130  
140  
150  
160  
170  
180  
190  
200  
210  
220  
230  
240  
250  
260  
270  
280  
290  
300  
310  
320  
330  
340  
350  
360  
370  
380  
390  
400  
410  
420  
430  
440  
450  
460  
470  
480  
490  
500  
510  
520  
530  
540  
550  
560  
570  
580  
590  
600  
610  
620  
630  
640  
650  
660  
670  
680  
690  
700  
710  
720  
730  
740  
750  
760  
770  
780  
790  
800  
810  
820  
830  
840  
850  
860  
870  
880  
890  
900  
910  
920  
930  
940  
950  
960  
970  
980  
990